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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,592	10/22/2003	Genichi Tanaka	027260-679	6371

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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,592	TANAKA, GENICHI	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Azm. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/7/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Synopsys design compiler tools in view of "Introduction to ASIC Design Methodology".

3. As per claim 1, Synopsys teaches a comprehensive circuit design tool comprising timing information generating apparatus for generating timing information on a functional block, said timing information generating apparatus comprising a library ("Design Compiler Technology Backgrounder", Introduction Section on page 2, standard cell or gate-array libraries) in which cells used for designing the functional block are registered ("Design Compiler Technology Backgrounder", Introduction Section on page

2); the logical connection information ("Design Compiler Technology Backgrounder", Report Generation section on pages 11, netlist, text file describing or representing a circuit block being designed) describing connection relationships between circuit components constituting the functional block, between the circuit components and the input pins and between the circuit components and the output pins ("Design Compiler Technology Backgrounder", Report Generation section on pages 11); generating timing information on a functional block, comprising of calculating delay times between any two nodes within the circuit design, in accordance with timing constraint information ("DC Ultra Technology Backgrounder", Register Retiming Section on pages 8-11, Figures 6-7 on page 8, setting the timing constraint of 10ns as the optimization goal and Synopsys then optimize timing of the circuit design in accordance to the timing constraint); and a timing information output unit (report generating) for outputting the timing information ("Design Compiler Technology Backgrounder", Report Generation section on pages 11).

Synopsys does not expressly teach said comprehensive circuit design tool comprising an input/output information identifying unit for identifying intra-block input stage sequential circuits and intra-block output stage sequential circuits by comparing logical connection information with a library; said intra-block input stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block input stage sequential circuits outside said functional block through input pins, said intra-block output stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block output stage sequential circuits outside said functional block through output pins; a delay time calculating unit

for calculating first delay times from the input pins to the intra-block input stage sequential circuits and second delay times from said intra block output stage sequential circuit to said output pins; and output timing information include the first delay times and the second delay times; and

does not expressly teach that the functional block is not complete as the design has not yet been completed.

Introduction to ASIC Design Methodology teaches a design methodology wherein the calculation of timing is carried out for the design of a function block that is not complete as the design process has not reach the chip production phase (Figure 1 on page 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Introduction to ASIC Design Methodology's design methodology into Synopsys' design tool.

The resulting combination of the references teaches that Synopsys design tool would have further comprises an input/output information identifying unit for identifying intra-block input stage sequential circuits and intra-block output stage sequential circuits by comparing logical connection information with a library, because it is well known in the art for circuit simulation tools such as Synopsys to generate a netlist, said netlist comprise of circuitry details such as the interconnection information and the cells utilized for the design. As the cells within the library contain the simulation information for said cell, it would have been obvious to then compare the netlist and the cell library in order to know which specific cells are utilized for the design, thus gaining the

necessary simulation information for simulating the circuit design; said intra-block input stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block input stage sequential circuits outside said functional block through input pins, said intra-block output stage sequential circuits being placed in the functional block and contributing to information exchange with extra-block output stage sequential circuits outside said functional block through output pins, because it is well known to one skilled in the art that data or information are exchanged among the plurality of circuit blocks and the specific boundary of the function block or circuit block along with the definition of the input and output pins for said function block or circuit block are predefined by the design requirement or the circuit designer; a delay time calculating unit for calculating first delay times from the input pins to the intra-block input stage sequential circuits and second delay times from said intra block output stage sequential circuit to said output pins, because Synopsys is able to calculate delay time between any two nodes within the circuit design, in order to implement improvements such as the timing optimization; and output timing information including the first delay times and the second delay times, because Synopsys is capable of generating a reporting after the timing optimization in order for analysis and possibly further optimization or correction; and further more, the functional block is in the incomplete phase, as the function block has not reach the chip production phase.

Therefore, it would have been obvious to combine Introduction to ASIC Design Methodology with Synopsys as the design methodology of the typical ASIC is well

known to one skilled in the art and the chart provide the appropriate design flow for produce a functioning chip.

4. As per claim 2, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 1 as discussed above, where Synopsys further teaches the setting of the delay time such that all input and output pins satisfy conditions described in the timing constraint information ("DC Ultra Technology Backgrounder", Figures 6-7 on page 8).

5. As per claims 3-4, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 1 as discussed above, and further more, since the spare time for the input and output pins can be determined uniformly or individually by a user from experience (such as an experience circuit designer), in combination with Synopsys' timing delay calculation and timing optimization and the ability for an experience circuit designer to setup an appropriate simulation and optimization for individual pins or group of pins, the delay time calculation unit sets (setting by delay calculation) the first delay time and the second delay time such that the input pins and output pins satisfy conditions described in the timing constrain information with leaving a same or different spare times for the input pins and output pins ("DC Ultra Technology Backgrounder", Figures 6-11 on pages 8-10).

6. As per claims 5-6, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 1 as discussed above, and further more, since the shortage of time for the input pins and the output pins can be determined uniformly or individually by a user from experience (such as an experience circuit designer), in combination with Synopsys' timing delay calculation and timing optimization and the ability for an experience circuit designer to setup an appropriate simulation and optimization for individual pins or group of pins. It would have been obvious that the delay time calculation unit sets (setting by delay calculation) the first delay time and the second delay time such that the input pins and output pins dissatisfy conditions described in the timing constrain information with leaving a same or different shortage of time for the input pins and output pins ("DC Ultra Technology Backgrounder", Figures 6-11 on pages 8-10).

7. As per claims 7-9, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 1 as discussed above, and further more, since the cells for driving the output pins can be uniformly or individually determined by a user from experience (such as an experience circuit designer), in combination with the Synopsys' cell library. It would have been obvious for the driving cell unit to specify (after the appropriate cells have been selected by the circuit designer from the cell library) a same cell or appropriate cells for all or each individual output pins. For example, a circuit designer may add inverter cells to reduce the delay time between two nodes, wherein the delay time is the resulting analysis from claim 1. Wherein larger the inverter cell

provides more drive and smaller inverter cell provide lesser drive. Such modifications obviously must not violate the design goals that were initially set up for the circuit block and the same or different appropriate standard cells are selected for the input and output pins, in accordance to the design goals. The Location Based Optimization (LBO) in Synopsys can also implement similar result ("DC Ultra Technology Backgrounder", Advanced Layout-Based Optimization section and Figures 12-13 on pages 15-18).

8. As per claims 10-13, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 7 as discussed above, and further more, since the user (such as an experience circuit designer) can decide the intra-functional block load capacitance of the input pins and the output pins uniformly or individually from experience, in combination with Synopsys' ability to output a netlist for back annotation, wherein said netlist includes parasitic capacitance for all metal wires interconnections, including the interconnections between the input and output pins ("DC Ultra Technology Backgrounder", Advanced Layout-Based Optimization section on pages 15-18) and it is well know that the parasitic capacitance associated with each output and input pins can be same or different for all of them, depending on the physical designed environment comprising parameters such as the length of the wire, the width of the wire and the specific layout location of the wire. It would have been obvious to further comprise a load capacitance specifying unit (after the appropriate load capacitance have been selected by the experienced circuit designer) for specifying a same uniform capacitance

or an appropriate individual capacitance for the input and the output pins as the intra-functional block load capacitance for the input and output pins.

9. As per claim 14, Synopsys and Introduction to ASIC Design Methodology teach all the limitations of claim 1 as discussed above, wherein as Synopsys is a comprehensive simulation tool for designing circuits, therefore, depending on how the circuit blocks are initially defined and broken down for either parallel or top-down implementation. A circuit block to be designed can have plurality of objects as claimed in claim 1 or a single object as claimed in claim 14. Therefore, since Synopsys is capable of implementing the timing analysis and outputting the calculation result as stated in claim 1 for a plurality of objects, Synopsys will also be capable of implementing the timing analysis and outputting the calculation result for a single object as claimed in claim 14.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
07/03/2004

Fritz Fleming

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